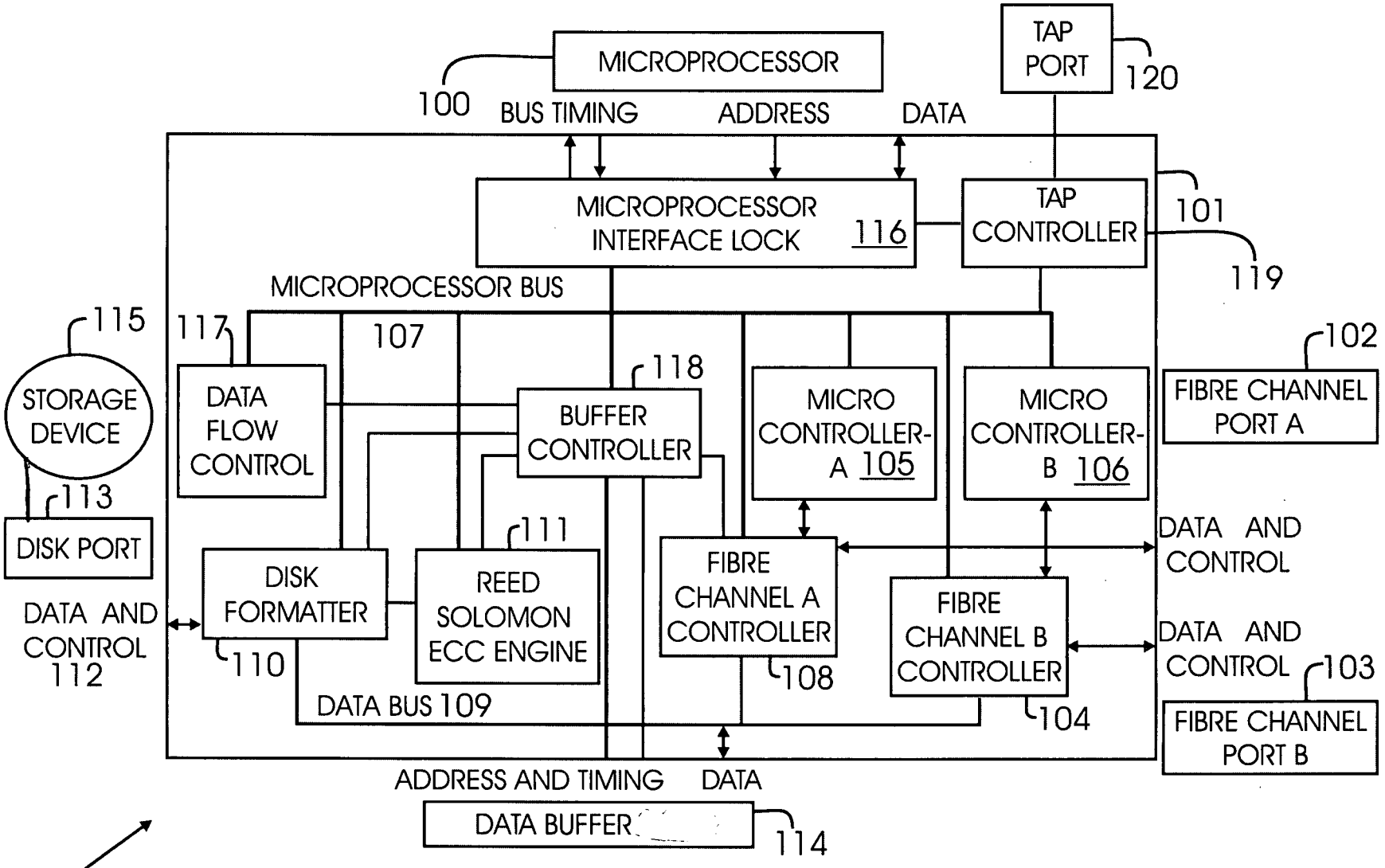
MICROPROCESSOR
100
BUS TIMING
ADDRESS
DATA
TAP PORT
120
MICROPROCESSOR INTERFACE LOCK 116
TAP CONTROLLER
101
119
MICROPROCESSOR BUS
115
117
107
118
102
STORAGE DEVICE
DATA FLOW CONTROL
BUFFER CONTROLLER
MICRO CONTROLLER-A 105
MICRO CONTROLLER-B 106
FIBRE CHANNEL PORT A
113
DISK PORT
111
DATA AND CONTROL
DISK FORMATTER
REED SOLOMON ECC ENGINE
FIBRE CHANNEL A CONTROLLER
FIBRE CHANNEL B CONTROLLER
DATA AND CONTROL
112
110
108
DATA AND CONTROL
103
DATA BUS 109
104
FIBRE CHANNEL PORT B
ADDRESS AND TIMING
DATA
DATA BUFFER
114
100A

FIGURE 1A

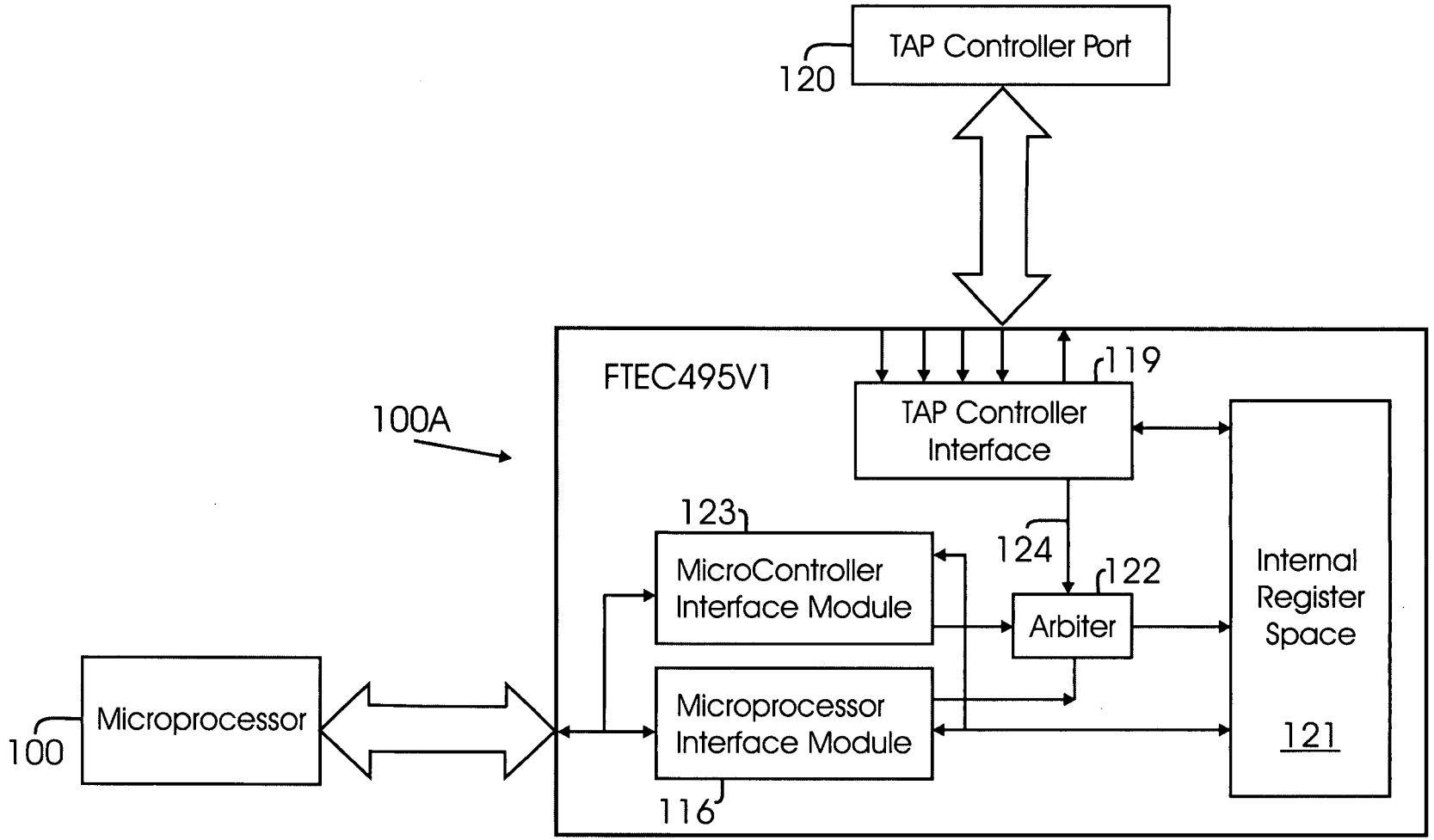
TAP Controller Port
120
FTEC495V1
119
100A
TAP Controller
Interface
123
124
122
MicroController
Interface Module
Arbiter
Internal
Register
Space
121
Microprocessor
100
Microprocessor
Interface Module
116

FIGURE 1B

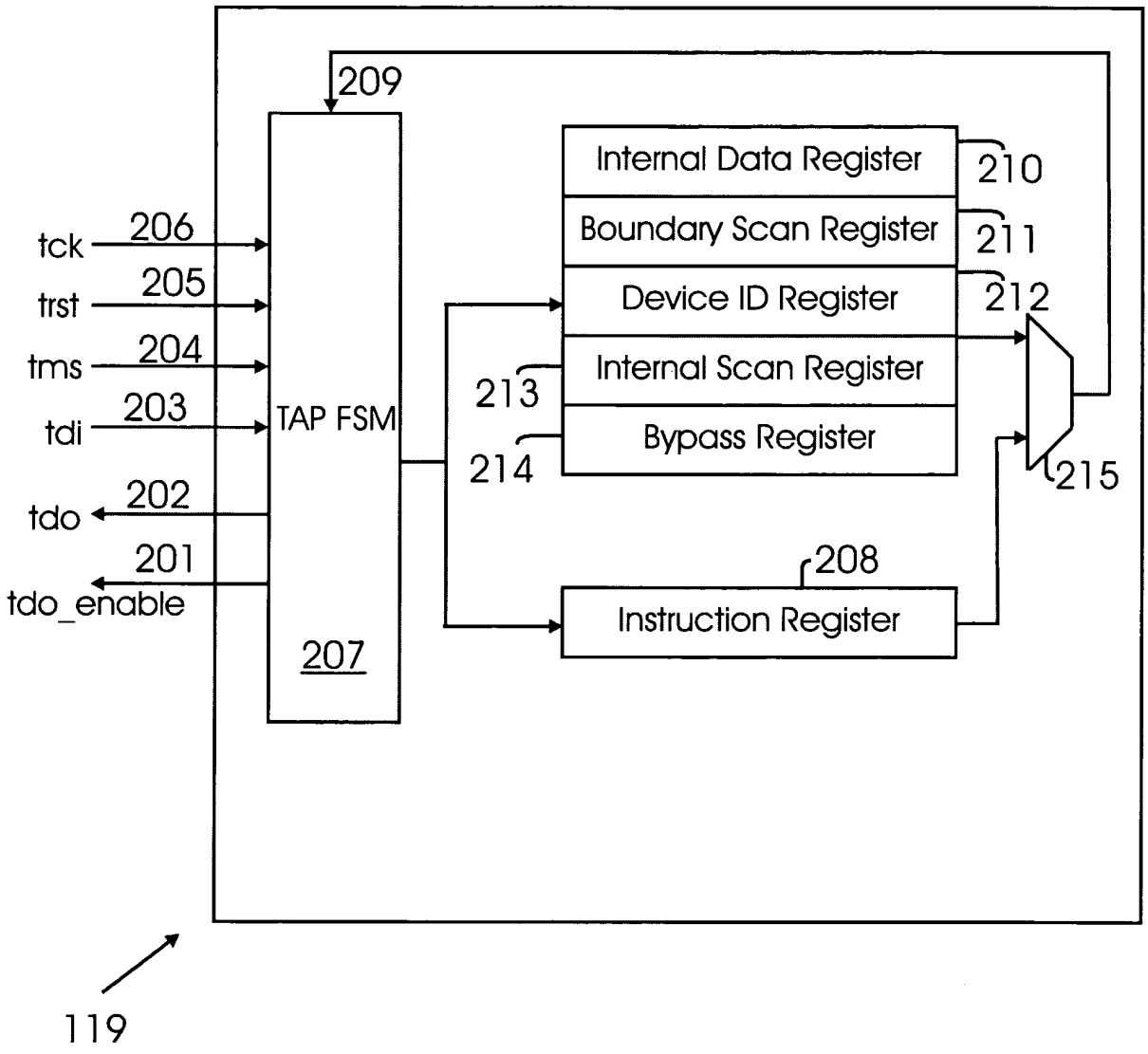
209
Internal Data Register
210
Boundary Scan Register
211
Device ID Register
212
Internal Scan Register
213
Bypass Register
214
215
tck
206
trst
205
tms
204
tdi
203
tdo
202
tdo_enable
201
TAP FSM
207
208
Instruction Register
119

FIGURE 2

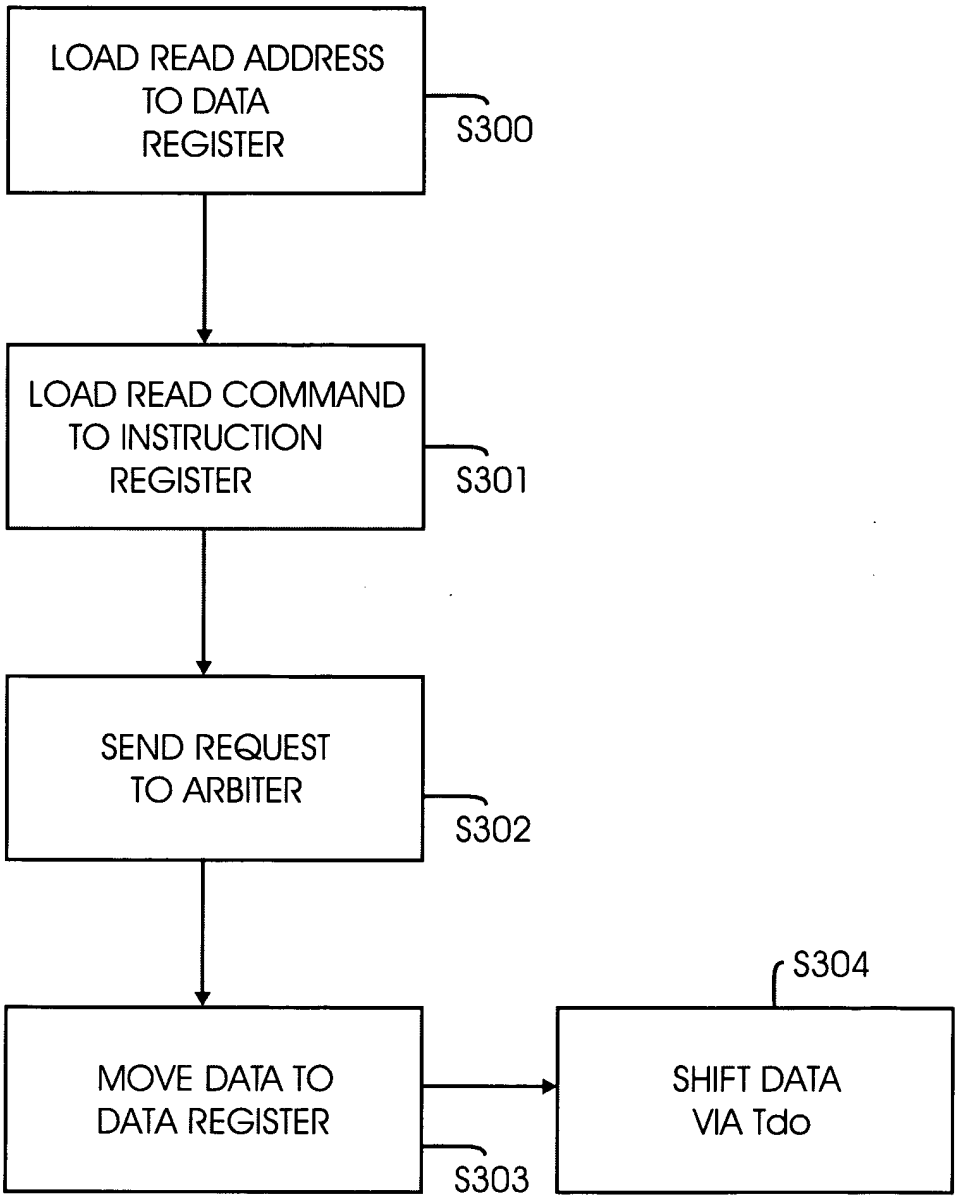
LOAD READ ADDRESS TO DATA REGISTER
S300
LOAD READ COMMAND TO INSTRUCTION REGISTER
S301
SEND REQUEST TO ARBITER
S302
MOVE DATA TO DATA REGISTER
S303
SHIFT DATA VIA Tdo
S304

FIGURE 3

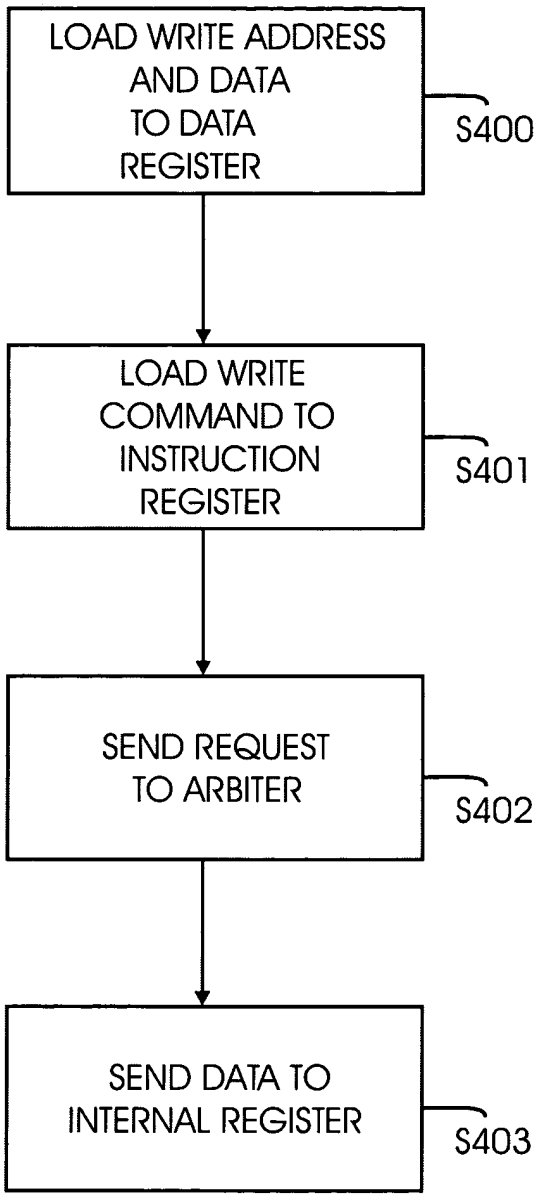
LOAD WRITE ADDRESS AND DATA TO DATA REGISTER
S400
LOAD WRITE COMMAND TO INSTRUCTION REGISTER
S401
SEND REQUEST TO ARBITER
S402
SEND DATA TO INTERNAL REGISTER
S403

FIGURE 4